

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 09-306159

(43)Date of publication of application : 28.11.1997

(51)Int.Cl.

G11C 7/00
G11C 7/00
G06F 1/26
G06F 1/32
G11C 11/401

(21)Application number : 08-142357

(71)Applicant : NIPPON TELEGR & TELEPH
CORP <NTT>

(22)Date of filing : 14.05.1996

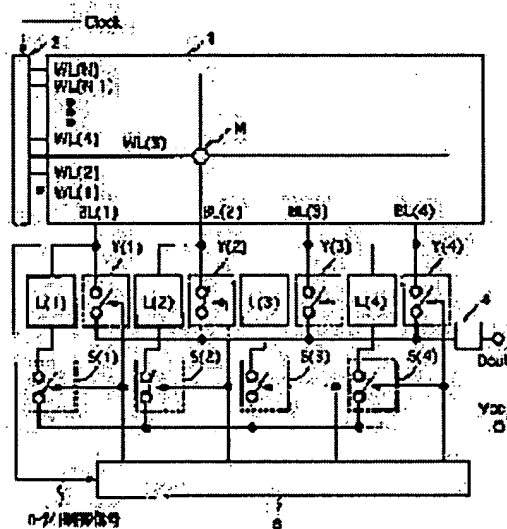
(72)Inventor : SHIBATA SHINTARO

(54) SEQUENTIAL READING MEMORY

(57)Abstract:

PROBLEM TO BE SOLVED: To control the load resistance of a bit line and to greatly reduce the power consumption by pulling up only the selected bit line by the load resistance and providing the means which separates a anon-selected bit line from a power supply.

SOLUTION: When a word line WL (3) and a bit line BL (2) are selected, a conventional switch S (2) is controlled in a conductive condition and signal voltages corresponding to the stored contents appear across a load resistor L (2). By detecting the voltages by a reading circuit 4, the stored contents are read to the external. However, in the embodiment, remaining switches S (1), S (3) and S (4) are controlled into a non-conductive state, no current flows into a memory cell from a power supply Vcc through load resistors L (1), L (3) and L(4). Thus, the power corresponding to the current is reduced.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]